CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor device, comprising:

selectively implanting a first region in a substrate so as to induce stress in a second region in the substrate; and

forming an electrical device in the substrate, at least a portion of the electrical device being in the second region.

2. The method of claim 1, wherein selectively implanting the first region comprises implanting the first region beneath at least a portion of the second region.

3. The method of claim 1, wherein selectively implanting the first region comprises:

forming a mask over a first portion of a top of the substrate so as to leave a second portion thereof exposed; and

performing an ion implantation using the mask so as to implant the first region in the substrate below the exposed second portion.

4. The method of claim 3, wherein selectively implanting the first region comprises implanting the first region beneath at least a portion of the second region.

5. The method of claim 3, wherein the mask comprises a dopant mask, and wherein forming the electrical device in the substrate comprises selectively doping the substrate using at least one of diffusion and implantation using the mask.

6. The method of claim 5, wherein selectively doping the substrate comprises forming at least one of a source/drain region and a channel region,

and wherein the second region comprises the at least one of the source/drain region and the channel region.

7. The method of claim 3, wherein the mask comprises an isolation mask, and wherein forming the electrical device in the substrate comprises selectively etching an isolation trench using the mask.

8. The method of claim 7, wherein performing the ion implantation comprises using at least one of carbon, germanium, and oxygen using the mask to implant the first region in the substrate below the exposed second portion.

9. The method of claim 5, wherein performing the ion implantation comprises using at least one of carbon, germanium, and oxygen using the mask to implant the first region in the substrate below the exposed second portion.

10. The method of claim 3, wherein performing the ion implantation comprises using at least one of carbon, germanium, and oxygen using the mask to implant the first region in the substrate.

11. The method of claim 10, wherein performing the ion implantation comprises implanting carbon in the first region so as to create a tensile stress in the first region.

12. The method of claim 10, wherein performing the ion implantation comprises implanting one of germanium and oxygen in the first region so as to create a compressive stress in the first region.

13. The method of claim 12, wherein performing the ion implantation comprises implanting one of germanium and oxygen in the first region so as to induce a compressive stress in the second region.

14. The method of claim 12, wherein performing the ion implantation comprises implanting one of germanium and oxygen in the first region so as to induce a tensile stress in the second region.

15. A semiconductor device, comprising:

first and second regions in a substrate, the first region begin implanted so as to induce stress in the second region; and

an electrical device, at least a portion of the electrical device being formed in the second region.

16. The semiconductor device of claim 15, wherein the first region is located beneath at least a portion of the second region.

17. The semiconductor device of claim 15, wherein the electrical device comprises at least one of a source/drain region and a channel region formed within the second region.

18. The semiconductor device of claim 15, wherein the first region is implanted with at least one of carbon, germanium, and oxygen so as to induce stress in the second region.

19. The semiconductor device of claim 18, wherein the first region is implanted with carbon so as to create a tensile stress in the first region.

20. The semiconductor device of claim 19, wherein the first region is implanted with one of germanium and oxygen so as to create a compressive stress in the first region.

21. The semiconductor device of claim 20, wherein the implantation of the first region with one of germanium and oxygen induces a compressive stress in the second region.

22. The semiconductor device of claim 20, wherein the implantation of the first region with one of germanium and oxygen induces a tensile stress in the second region.

23. A method of improving carrier mobility in a channel region of a MOSFET device, comprising:

implanting a first region in a substrate so as to induce stress in a second region in the substrate; and

forming at least a portion of the channel region in the second region of the substrate.

24. The method of claim 23, wherein implanting the first region comprises implanting at least one of carbon, germanium, and oxygen so as to induce stress in the channel region.

25. The method of claim 24, wherein implanting a first region comprises inducing a compressive stress in the channel region.

26. The method of claim 24, wherein implanting a first region comprises inducing a tensile stress in the channel region.

27. The method of claim 23, wherein implanting the first region comprises implanting the first region with carbon so as to create a tensile stress in the first region.

28. The method of claim 23, wherein implanting the first region comprises implanting the first region with one of germanium and oxygen so as to create a compressive stress in the first region.